

ABSTRACT OF THE DISCLOSURE

A latch based random access memory includes an input data register; an input data buffer coupled to the input data register; a latch array coupled to the input data buffer; and a latch array bypass multiplexer for selecting one of the input data buffer and the latch array in response to a memory scan mode signal to generate a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing.